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Summary
Report

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DEVELOPMENT AND FABRICATION OF A MOLECULAR ELECTRONICS PREAMPLIFIER

December 21, 1964

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S U M M A R Y R E P O R T

WS-116 NASA PRE-AMPLIFIER

CONTENTS

I Introduction

The WS-116 is designated a pre-amplifier. Perhaps it is more descriptive to use the term "controlled output current switch." Its basic function is illustrated in Figure 1. The pre-amplifier is used to convert a logical "one" output from a flip flop into a one ampere pulse. This pulse in turn saturates a power transistor which delivers a high current pulse (10 amperes) to a transformer.

For optimum performance, the pre-amplifier output current should be high enough to fully saturate the power transistor but should not greatly "overdrive" it as this would increase switching times. In addition, it is necessary to operate over the entire temperature range -55 to +125°C and turn-on and turn-off times should be on the order of .25 μ sec. A further restriction on the pre-amplifier is the severe power limitation of our present integrated circuit stud package 15°C/watt.

To meet the above requirements, the pre-amplifier circuit of Figure 2 was chosen. It is a simple means of approaching a constant output current switch, "triggered" by a minimum voltage-current input but relatively insensitive to higher voltage inputs or large temperature changes. Because both Darlington transistors are normally unsaturated and "excess" input current is shunted, the switching time is relatively constant with respect to input conditions.

A composite drawing of the device geometry is shown in Figure 7. Also included is the complete circuitry of the dual device.

The basic principle of operation is that the Darlington input is shunted by three forward biased diodes. At low input voltage and hence very low current through the forward biased diodes this shunt impedance is very high. As the input voltage approaches the VBE of the Darlington for one

ampere collector current, the shunt begins to conduct appreciably and its impedance decreases rapidly (for a forward biased diode $R_D \approx \frac{kT}{qID}$). Slightly above one ampere Darlington current, the diode shunt is drawing enough current through Rs so that it essentially shunts out any "excess" input signal. The diode shunt is effective over a wide temperature range because the temperature coefficient of two of the shunt diodes matches the Darlington diodes and the third diode varies in the opposite manner as the current gain of the Darlington. A detailed analysis is presented in a later section.

II Results

The initial target specifications desired by NASA are summarized in Table I. These specifications were later qualified to mean compatibility with an input signal consisting of a logic circuit output such as a flip flop; and a load transistor such as the 2N 1016.

The results obtained with the WS-116 are summarized in Table II and Figure 3. Average values per unit are used in Figure 3. The circuit used to simulate appropriate input and load conditions is shown in Figure 5. Two different input voltages were used to "bracket" various input signals. An "average" summary of results is shown below. It may be considered a "typical performance".

	Average Performance		
Temp	-55	25°C	+125
Vin = 3.0v			
I out, amps	1.20	1.40	1.10
t on, μsec.*	0.26	0.28	0.24
t off, μsec.*	0.18	0.22	0.18
Vin = 3.5v			
I out, amps	1.40	1.60	1.20
t on, μsec.	0.30	0.34	0.26
t off, μsec.	0.17	0.24	0.20

* Times refer to total current switched.

While the data variation between units (See Table II) is quite large the following general conclusions may be drawn.

(1) While maintaining a minimum current of 1 amp at -55°C, it is possible to hold the output current of the device well below 2 amps at higher operating temperatures.

(2) The average "propagation delay" or $(t_{on} + t_{off})/2$ is about 0.25 μ sec. at all temperatures for the total current switched.

(3) Propagation delay for switching 1 amp is about 0.20 μ sec. at all temperatures.

III Discussion of Results

A. Comparison with Target Specifications

(1) Output current

In general, the performance with respect to output current was very satisfactory. Only a rough control of current is required and Figure 3 shows this has been obtained. Variations in output current are due primarily to variations in Darlington current gain (hfe), and the internal emitter series resistance (Rse). A plot of output current versus current gain and temperature for two different input voltages is shown in Figure 4. At higher input voltages the very high gain units show a greater variation of output current with temperature thus putting an upper limit on the useful beta range.

In order to provide a basis for evaluation it becomes appropriate to compare the WS-116 with some of the more conventional means of current control. These are shown in Figure 6. One of the primary disadvantages of both techniques is the difficulty of obtaining precision 1.0 ohm integrated circuit resistors. Higher value resistors can be used if power consumption is not a problem and an adequate voltage is available. A preliminary study of both circuits indicates that with present integrated circuit techniques, the anticipated current control might be no better than that of the WS-116 and switching time would be much slower, since the available signal from a logic block is a very poor source to drive either circuit in Figure 6. A recent study of heavily doped resistors, which would be used for low values of resistance, indicates the following value of temperature coefficients. For the circuits of Figure 6 the

output current variation would be of this order of magnitude.

Temperature ^{o}C	-55	25	+125
Resistance Ratio	0.95	1.0	1.1

Of course, the best circuit choice depends a great deal on the details of the specific situation.

B. Switching Times

The turn-on and turn-off times obtained with the WS-116 compare favorably with the target specification. The values recorded in Table II and the "typical" values of the previous page refer to switching the total current. This gives a worst case value. Nevertheless, the average of the turn-on and turn-off times was close to 0.25 μ sec. under all conditions. Turn-on times were on the high side of the target. On the basis of the time required to switch 1 amp, the average was well under 0.25 μ sec. under all conditions.

C. Breakdown Voltage LVCEO

The LVCEO of the devices ranged from 8 to 17 volts, although the collector resistivity should have given much higher breakdowns. The low breakdowns are attributed to outdiffusion from the floating collector during subsequent processing. Recently we have been able to obtain very low sheet resistance in this diffusion, lower in fact than actually required. Backing off on the floating collector sheet resistivity should give much higher breakdowns, (other processing variables kept constant) with only a slight increase in saturation resistance.

D. Leakage Current ICEO at 5.0 volts

Although not specified initially, it is reasonable to assume a maximum desirable leakage current of about 100 μA. Routine processing should give leakage currents less than 10 μA.

E. Overall Darlington Current Gain - BETA

Since the diode shunt is a current "robbing" device, it is necessary to measure beta at a collector current level where the shunt is inoperative. One-tenth amp was chosen. As Table II and Figures 3 and 4 show, the useful beta range ($25^{o}C$ measurements) is from 3300 to about 20,000 depending on input voltage and minimum and maximum allowable output current. This represents an individual transistor gain of about 55 to 150, which seems like a reasonable processing goal.

A more optimum Darlington beta range would be 4000 to 6000. This requirement however, could reduce yields considerably.

F. Stud Package

Although a considerable effort was made to obtain a satisfactory six-lead package certain technical difficulties made it necessary to resort to a makeshift solution.

It is recommended that in the future a detailed investigation of the thermal impedance and mechanical strength of various packaging alternatives be undertaken before a final design is accepted for high power integrated circuit applications.

IV Future Applications

Effective current control by the diode shunt principle has been clearly demonstrated by this study. The following paragraphs explore the basic limitations of the device with regard to future applications.

A. Operating Voltage

The limitations are the LVCEO of the device and the requirement that the difference between input and output voltage be kept in the range of 2.5 to 3.5 volts. The diode shunt principle does not depend on the collector voltage and present techniques could be used to make devices operating in the 50 to 100 volt range.

B. Output Current Level

Theoretically it is possible to design around a center value of almost any magnitude of output current, and hold this value from unit to unit as well as over a wide range of temperature and input voltage conditions. Each case, however, would have to be considered separately since inserting resistances in the emitter, base or shunt legs might be required. It also may be expedient to increase the number of shunt diodes.

C. Output Current Control

As will be shown in Section V a rough approximation for output current is

$$I_{out} \simeq \beta V_F \; / \; (Rb + \beta \, Rse)$$

where β = darlington current gain, beta

V_F = diode forward drop

Rse = emitter series resistance inherent to the device.

To obtain a very narrow range of output current it is necessary to hold these parameters to the appropriate tolerances.

C. Output Current Control (contd.)

A balance must therefore be chosen between yield and output tolerances. Temperature variation may roughly be assumed as ±20% although Section V shows that several types of temperature variations may be obtained.

V Derivation of Expressions for Output Current

A. Expression for Output Current

A generalized circuit diagram for the preamp is shown in Figure 8. We are concerned with the currents flowing through the darlington versus the diode shunt as a function of input voltage, output current and temperature.

For the darlington:

$$V_{in} - V_{out} - I_{in}(R_{in} + R_s) = IbRb + Ib(rb' + \beta_1 Rse_1) + Ib_2(rb'_2 + \beta_2 Rse_2) + 2V_F^* + I_{out} R_e \quad (1)$$

where V_F = forward voltage drop of a diode

V_{in} = source input voltage

V_{out} = load voltage

R_{in} = source series resistance

Rse = device emitter series resistance.

To a first approximation, the darlington beta $\beta = \beta_1 \beta_2$, the product of the individual transistor betas. Neglecting rb' and assuming $Rse_1 \ll \beta_2 Rse_2$, $Ib(rb' + \beta_1 Rse_1) + Ib_2(rb'_2 + \beta_2 Rse_2) \approx Ib\beta Rse_2$. Or omitting the subscript $Ib\beta Rse$.

for the diode shunt:

$$V_{in} - V_{out} - I_{in}(R_{in} + R_s) = I_{shunt} R_g + 3V_F \quad (2)$$

Equating (1) and (2)

$$I_{shunt} = \frac{Ib\left[Rb + \beta(Rse + Re)\right] - V_F}{R_g} \quad (3)$$

* A correction factor can be inserted to allow for the fact that the base-emitter diode of the power transistor is conducting a very high current and therefore its forward drop is about 0.1 volts higher than a shunt diode.

Substituting in (2) and using $I_{in} = Ib + I_{shunt}$, $V_{in} - V_{out} - Ib(R_{in}+Rs) =$

$$Ib\left[\left[Rb + \beta(Rse + Re)\right]\left[1 + \frac{R_{in} + R_s}{R_g}\right]\right] - \left[V_F\right]\left[\frac{R_{in} + R_s}{R_g}\right] + 2V_F$$

Giving:

$$I_{out} = \beta\, Ib$$

$$= \beta \left[\frac{(V_{in} - V_{out} - 2V_F) + \left[V_F\right]\left[\frac{R_{in} + R_s}{R_g}\right]}{R_{in} + R_s + \left[Rb + \beta(Rse + Re)\right]\left[1 + \left[\frac{R_{in} + R_s}{R_g}\right]\right]} \right] \quad (4)$$

In an appropriately designed unit $\frac{R_{in} + R_s}{R_g} > 10$

and, equation (4) simplifies to

$$I_{out} = \beta \frac{V_F}{Rb + \beta(Rse + Re)} \quad (5)$$

B. Output Current Variation With Temperature

The following table of normalized values of β, V_F and Rb may be considered typical for integrated circuits.

Normalized Values

Parameter	Temp.	-55°C	25°C	+125°C
β		0.33	1.0	2.20
V_F		1.33	1.0	0.67
Rb		0.85	1.0	1.30
Rse + Re		1.00	1.0	1.00

The darlington beta varies roughly as the "square" of an individual transistor beta. Figure 9 is a normalized plot of I_{out} as calculated by Equation (5). Three curves are obtained for the assumptions:

$Rb \gg \beta (Rse + Re)$	all temp.
$\beta (Rse + Re) \gg Rb$	all temp.
$\beta (Rse + Re) = Rb$	$25^{o}C$

Figure 9 suggests the possibility of designing for several different types of variation of output current with temperature. It is interesting to contrast the curves of Figure 9 with those of Figure 3.

The design values for the WS-116 are as follows:

Temp.	-55	25	+125°C
Rb, ohms	640	750	1,000
β	2,000	6,000	13,200
Rse, ohms	0.25	0.25	0.25
V_F, volts	0.80	0.60	0.40
I_{out}, amps	1.40	1.60	1.25

The estimate calculated from the above parameter values by using Equation (5), gives a good "ballpark" figure. The accuracy of the estimate is somewhat misleading. For greater accuracy a more detailed calculation procedure is generally used.

In the WS-116 no additional Re was used, although this feature is desirable, because of the difficulty of obtaining the 0.1 to 0.5 ohm resistor values which would be required. In addition the shunt diode resistance was high enough without the use of a separate R_g. Re and R_g were included in the analysis for the sake of obtaining generality.

C. Output Current versus Input Voltage

A very important control feature is the relative independence of output current on input voltage. Equation (3) indicates the mechanism for this. Once the product Ib (Rb $+\beta$[Rse + Re]) exceeds V_F then the ration of shunt to base current approaches $\frac{I_{shunt}}{Ib} = \frac{[Rb + \beta(Rse + Re)]}{R_g}$

$= \gg 1.0$

In the WS-116, R_g is only the dynamic impedance of the diode kT/qI, and this resistance becomes quite small with only a moderate shunt current flowing. The shunt current does flow through the series resistance (R_{in} + R_s), producing a voltage drop which dissipates any "excess" input signal.

TABLE I

Target Specifications

Supply Voltage	4.0 Volts
Input Signal	4 volts and 5 ma
Output for above signal	1 ampere min
Delay plus rise of Output for a step input	0.25 μsec max.
Storage and fall time without back bias	0.25 μsec max.
Worst case design to meet specifications over temperature range	-55 to + 125°C

TABLE II

Summary of MS-116 Performance

Unit #		102		104		107		108		109		110		111		112	
Side (1)		A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
LVCEO min, V		12	12	8	8	8	8	8	17	14	12	10	11	10	10	10	9
ICEO @ 5V, μa		2	2	1	1	4	4	1	1	1	40	1	1	1	1	1	1
hfe @ 0.1A 2.5 V		3300	3300	3300	3300	5500	5500	5000	5000	3300	4000	3000	4000	6000	6000	10,000	10,000
Vin = 3.0V																	
	I out, amp	1.25	1.25	1.18	1.18	1.67	1.57	1.27	1.37	1.18	1.18	1.47	1.47	1.67	1.67	1.67	1.67
25°C	tr, μsec	.30	.30	.29	.28	.36	.36	.27	.28	.25	.24	.26	.28	.32	.32	.37	.32
	tf, μsec	.16	.16	.17	.28	.28	.16	.16	.16	.12	.12	.24	.24	.26	.26	.24	.22
	I out	.98	1.06	1.10	1.10	1.27	1.27	1.08	1.18	.79	.88	1.10	1.14	1.49	1.49	1.37	1.37
-55°C	tr	.26	.27	.25	.22	.28	.27	.25	.26	.18	.18	.22	.22	.30	.28	.30	.30
	tf	.14	.14	.14	.14	.24	.24	.14	.14	.08	.08	.18	.18	.22	.22	.20	.20
	I out	.94	.94	.90	.92	1.25	1.25	.90	.98	.98	.94	1.19	1.18	1.22	1.37	1.22	1.22
125°C	tr	.25	.24	.24	.24	.28	.26	.23	.23	.20	.20	.24	.24	.26	.28	.24	.24
	tf	.14	.15	.16	.17	.27	.27	.16	.16	.16	.16	.20	.20	.24	.24	.24	.22
Vin = 3.5V																	
	I out	1.37	1.37	1.37	1.37	1.86	1.86	1.37	1.57	1.37	1.47	1.67	1.67	1.86	1.86	1.86	1.86
25°C	tr	.33	.33	.33	.32	.44	.40	.30	.34	.28	.28	.34	.34	.44	.40	.42	.40
	tf	.14	.14	.18	.20	.32	.32	.19	.19	.16	.16	.24	.22	.26	.26	.24	.25

	I out	1.04	1.10	1.25	1.25	1.47	1.57	1.33	1.37	.94	1.00	1.25	1.41	1.76	1.76	1.57	1.57
-55°C	tr	.27	.28	.30	.28	.32	.34	.26	.27	.18	.18	.26	.26	.42	.42	.40	.36
	tf	.14	.14	.14	.14	.29	.27	.15	.15	.10	.10	.17	.17	.20	.20	.22	.22
	I out	.98	1.02	.94	.98	1.37	1.37	.98	1.05	1.10	.98	1.29	1.29	1.33	1.53	1.29	1.29
125°C	tr	.25	.24	.24	.25	.30	.30	.22	.22	.22	.22	.24	.27	.27	.32	.28	.26
	tf	.16	.16	.16	.17	.28	.28	.16	.16	.16	.16	.20	.20	.24	.24	.23	.24

(1) Dual Circuit—See Marking Diagram Fig .

(2) 0% to 90% or 100% to 10% for tr and tf respectively. Rise time is measured from the point of step input. Fall time is measured from the point of input pulse step fall.

TABLE II, SUPPLEMENT

Summary of Performance
Additional Units

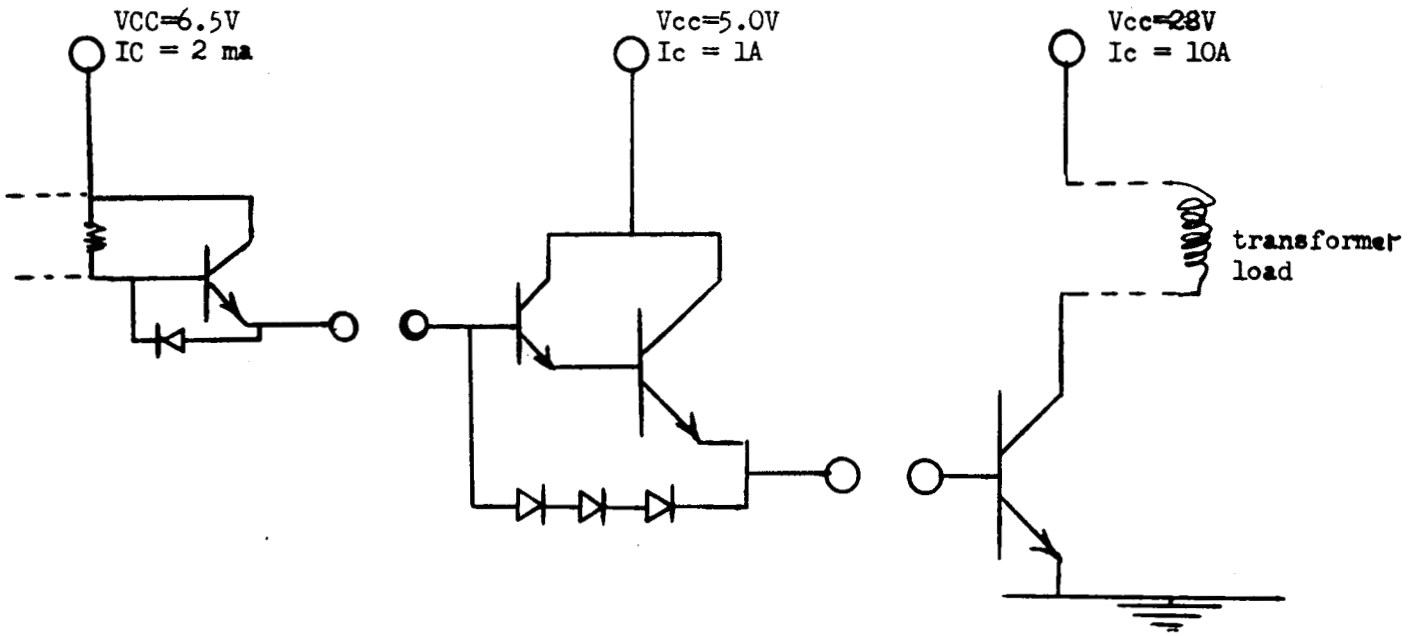
		200		201 X		202		203		204		205 X		206	
Side		A	B	A	B	A	B	A	B	A	B	A	B	A	B
LVCEO min, V		8.0	8.5	7.5	8.0	7.0	7.0	10.0	16.0	15.0	10.0	8.5	9.0	8.5	8.5
ICEO @ 5V, ua.		4	10	1600	< 1	< 1	< 1	< 1	< 1	70	1	900	5	< 1	< 1
B @ 100 ma 2.5V		20,000	20,000	20,000	20,000	8000	8000	4000	4000	4000	4000	10,000	10,000	16,000	18,000
	Temp. °C														
3.0V Vin	-55	1.90	1.90	1.70	1.70	1.50	1.60	1.28	1.28	1.04	1.04	1.60	1.72	1.80	1.70
	I out, Amp 25	1.60	1.56	1.48	1.44	1.52	1.50	1.34	1.28	1.24	1.20	1.60	1.50	1.50	1.40
	125	1.04	1.00	1.08	1.04	1.08	1.00	0.96	0.84	0.84	0.76	1.12	1.04	0.96	0.88
3.5V Vin	-55	2.10	2.10	2.00	2.00	1.74	1.80	1.40	1.40	1.26	1.20	1.90	1.96	2.10	1.96
	I out, Amp 25	1.80	1.80	1.90	1.80	1.80	1.16	1.60	1.50	1.36	1.28	1.80	1.80	1.60	1.60
	25	1.20	1.20	1.20	1.16	1.14	1.08	1.08	1.92	0.88	0.84	1.20	1.16	1.08	1.00

	207		208		209		210		211		212	
	A	B	A	B	A	B	A	B	A	B	A	B
LVCEO	8.0	7.5	18.0	22.0	8.0	8.0	18.0	18.0	8.0	8.0	8.5	7.5
ICEO @5V	10	< 1	500	< 1	15	< 1	< 1	< 1	25	320	< 1	120
B @ 100 ma 2.5V	15000	15000	3000	3000	8000	8000	3000	2500	8000	10000	14000	18000
Temp. °C												
3.0V Vin -55	1.72	1.56	0.90	0.92	1.44	1.48	0.96	0.94	1.48	1.34	1.76	1.54
I out, Amp 25	1.60	1.92	1.10	1.16	1.44	1.40	1.16	1.08	1.52	1.44	1.72	1.60
125	1.12	2.00	0.80	0.80	1.12	1.04	0.80	0.84	1.04	0.96	1.00	1.00
3.5V Vin -55	2.20	2.30	1.02	1.04	1.60	1.60	1.08	1.04	1.70	1.54	2.10	2.00
25	1.80	2.20	1.20	1.20	1.70	1.70	1.28	1.20	1.70	1.50	1.70	1.70
125	1.24	2.00	0.90	0.88	1.16	1.08	0.92	0.92	1.16	1.08	1.16	1.16

X These units were not delivered to NASA.

Fig. 1

WS-116, System Function

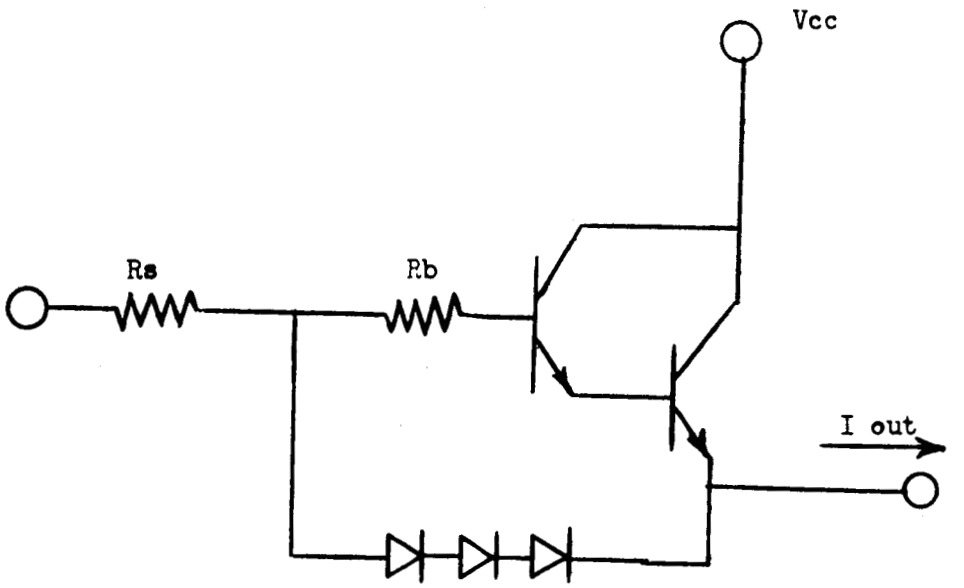


	Logic block (1)	Preamplifier	Power Transistor
Nominal output	1 ma @ 4V	1A @ 1V	10A

(1) Emitter-follower (high fan out) portion of logic system is shown

Fig. 2

WS-116 Circuit Diagram (1)



(1) The WS-116 is a dual circuit so the above diagram is one half of the total functional block. See Fig. 7

FIGURE 3

Output Current vs Temperature
and Input Voltage

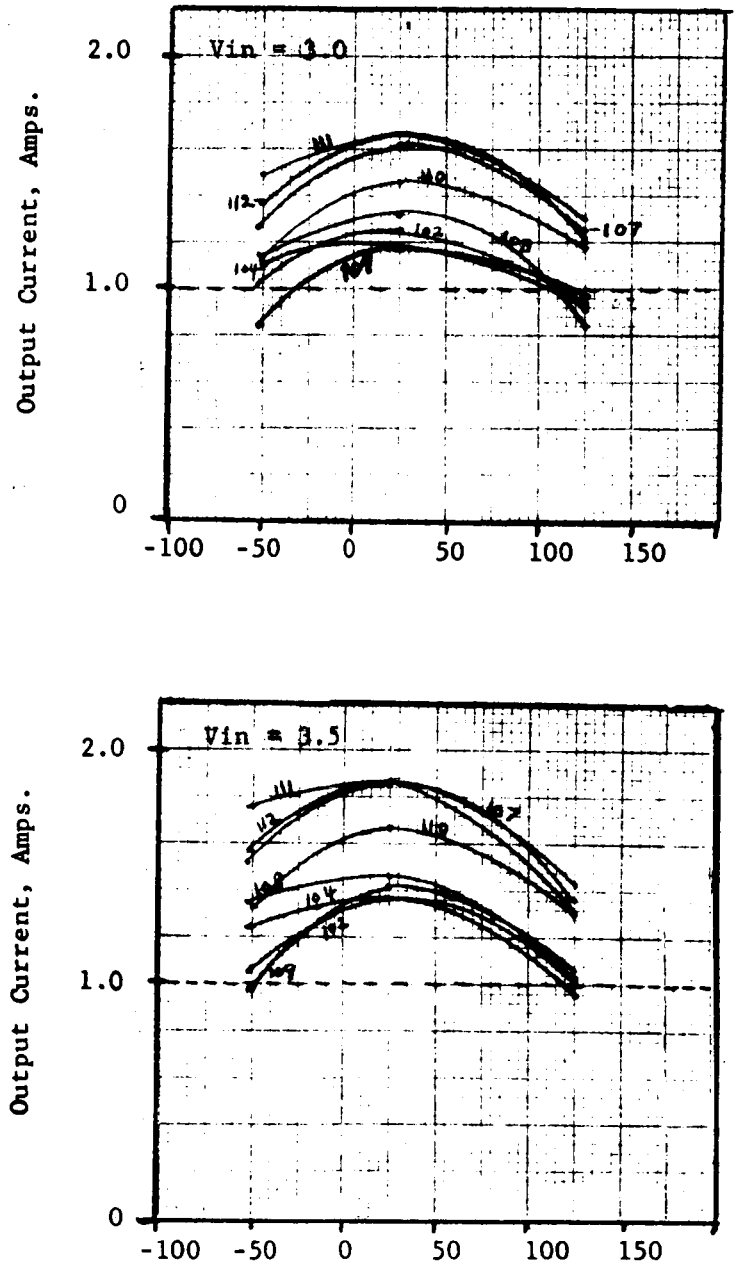


FIGURE 4

Output Current vs Darlington Beta

Input Voltage and Temperature

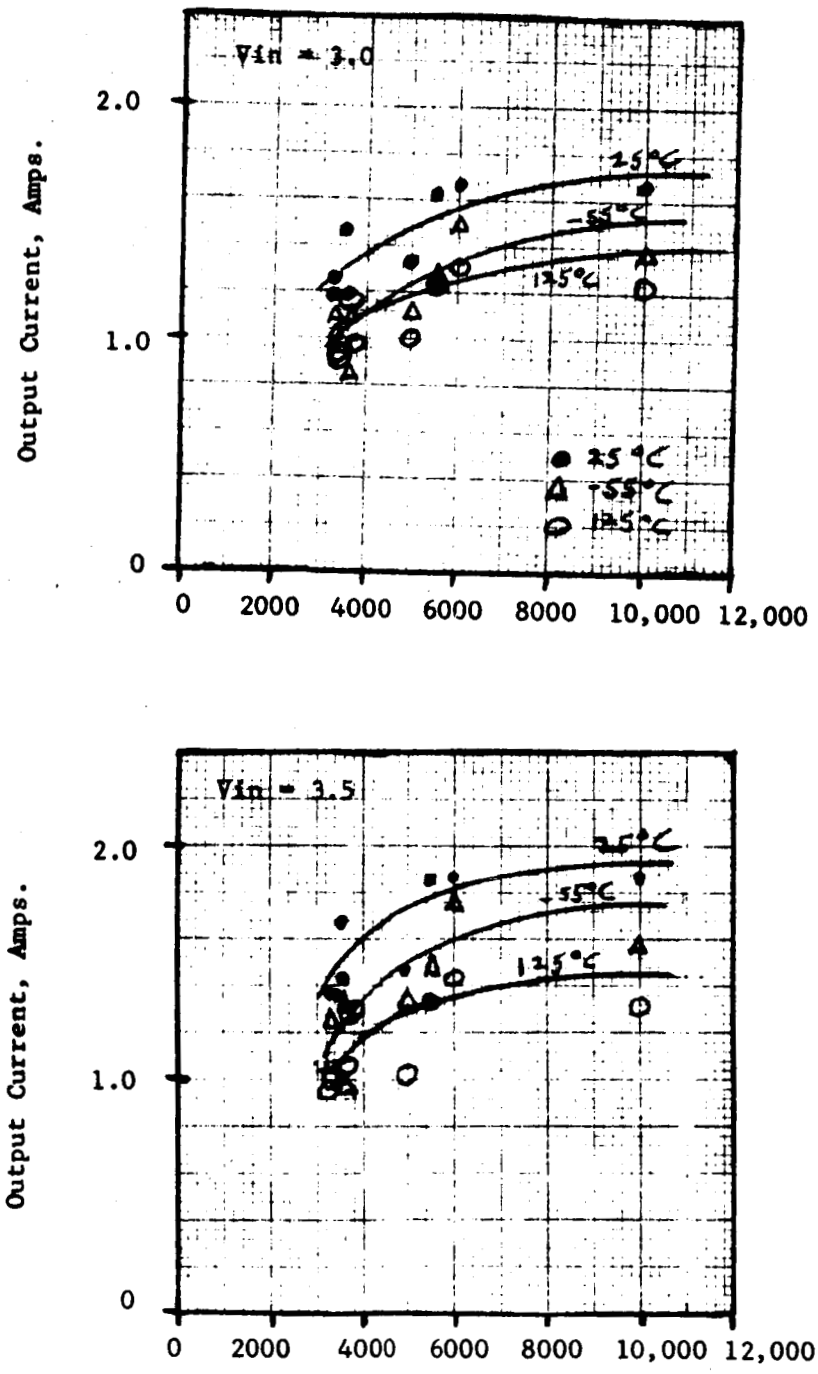
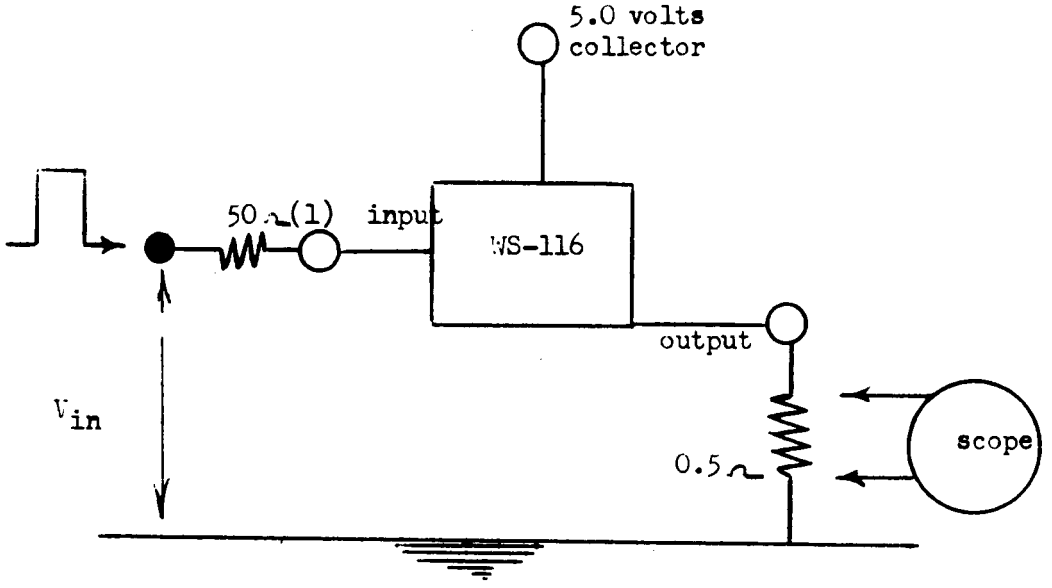


Fig. 5

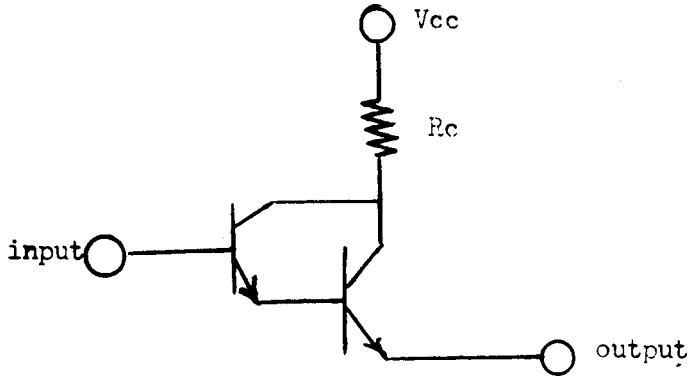
Test Circuit

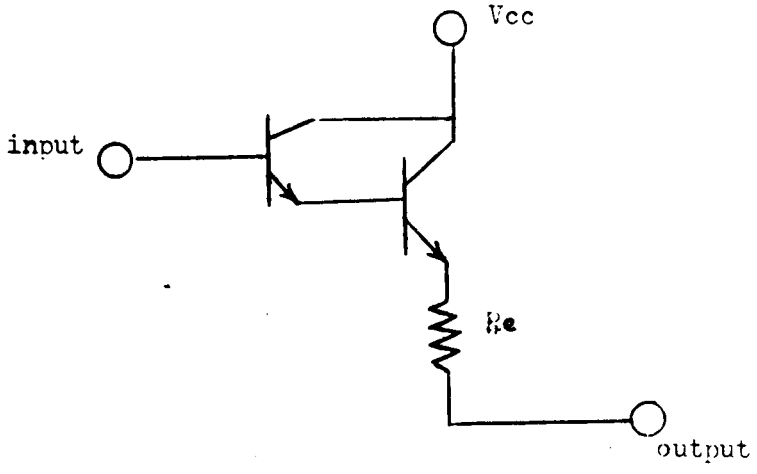


(1) Simulates the minimum series resistance of a logic device output.

Fig. 6

Conventional means of current control





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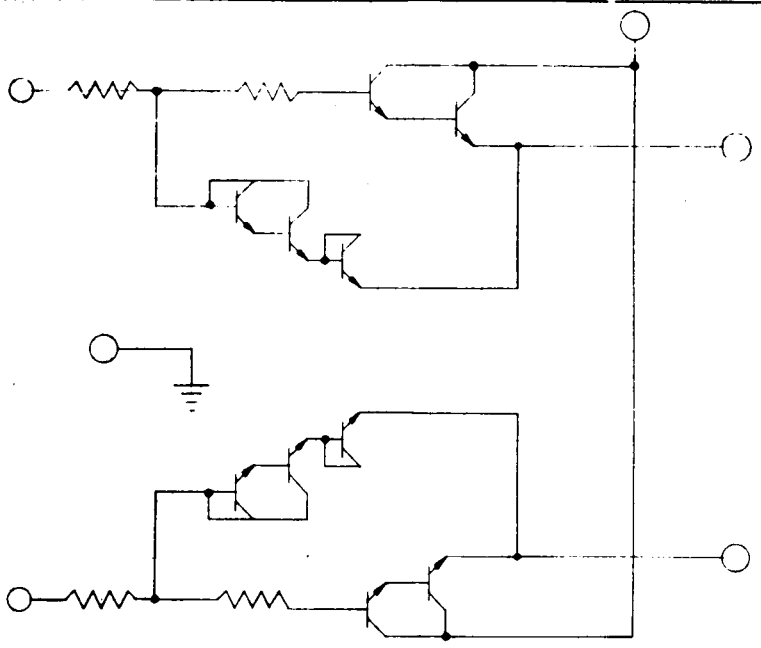
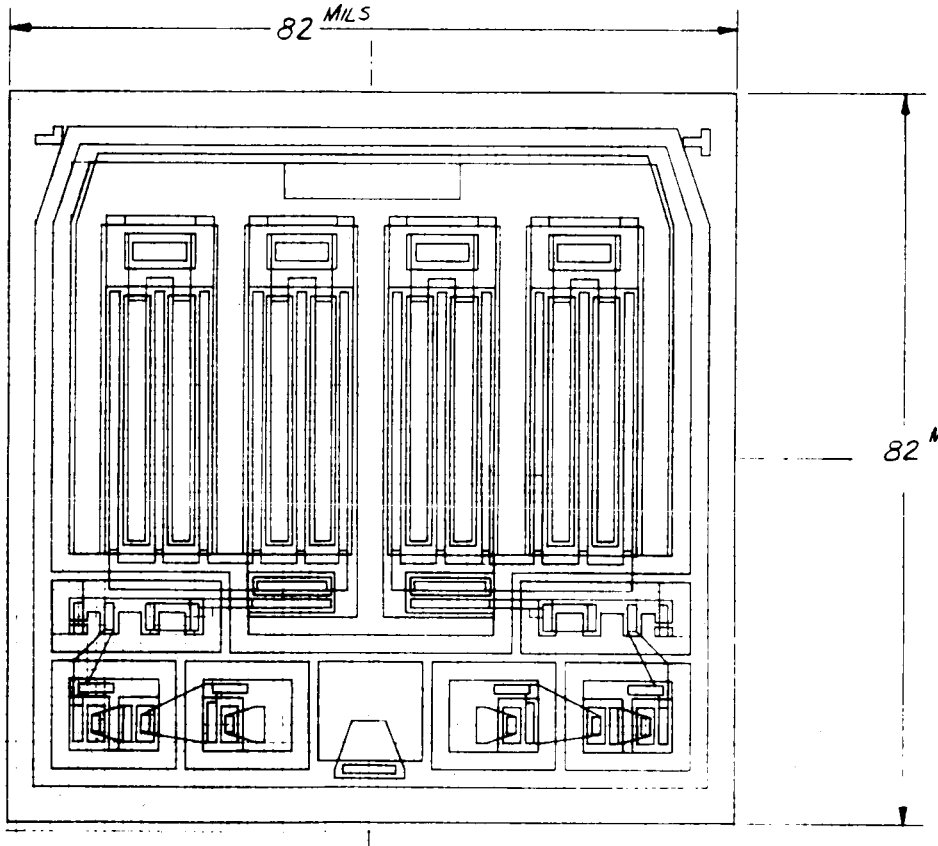




ALL LINES NOT ON GRID ARE .5 MILS

B	1	CHG MASKS #3, 4, 5, 6, 7. CHG LET "B" ON ALL MASKS P.F. 5/9/69
A		OPENING IN N+ DIFFUSION ENLARGED. MASK #1 CHANGED SLH 1/31/64
LTR	CHANGE	

WESTINGHOUSE ELECTRIC CORPORATION

TITLE NASA PREAMPLIFIER

NAS8-5455 WS 116

DIMENSIONS SQUARE 1 MIL SUB. 1

DRWN HESS, G. 1/29/64 APPD

CHKD APPD

SUPV. APPD

3123C18 SHEET 1 OF 1

REF DRG

LOCATION MOLECULAR ELECTRONICS DIVISION ELKRIDGE BALTIMORE 3, MARYLAND

FIGURE 8

Generalized Circuit Diagram

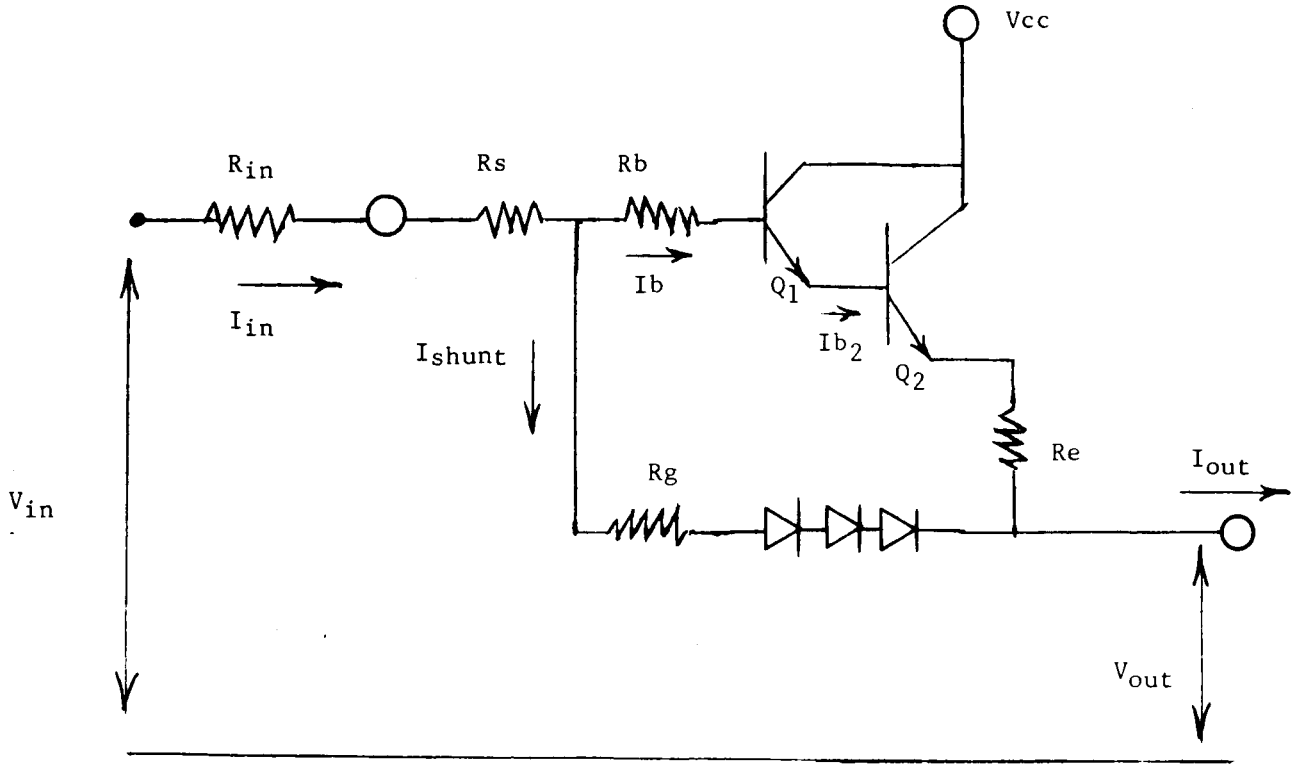


FIGURE 7

Normalised Output Current vs Temperature

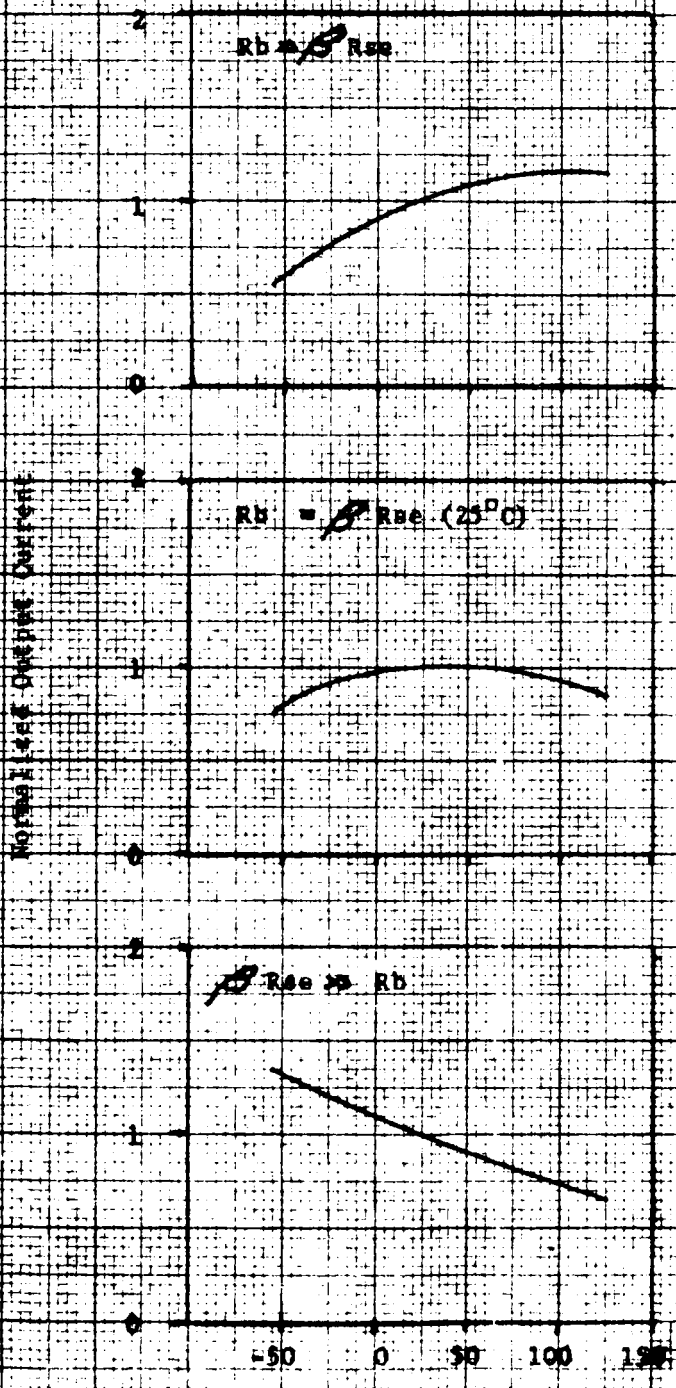
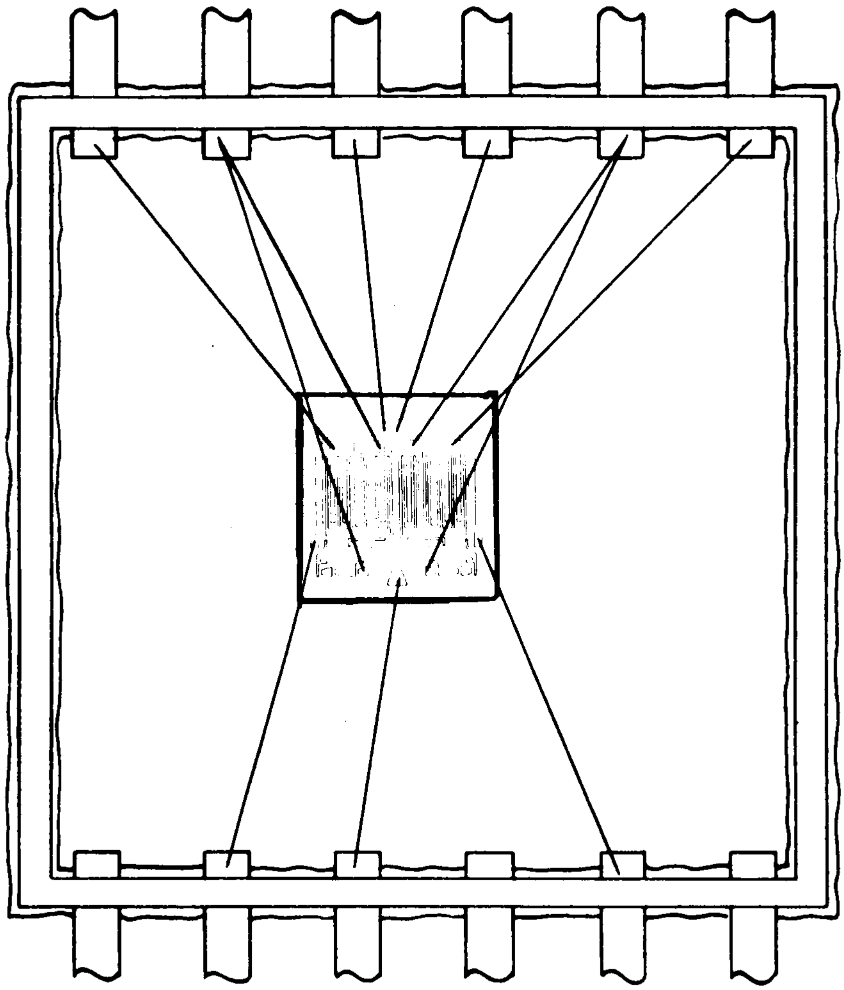


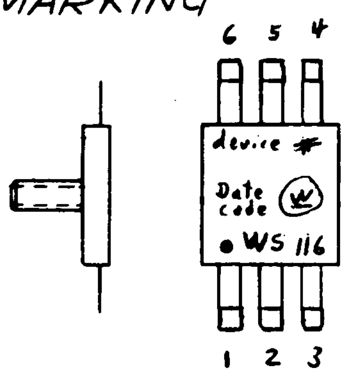
FIG 10

(W) MOLECULAR ELECTRONICS DIVISION - PROPRIETARY CLASS 2
LOCATION : ____________________

WIRING



MARKING



PRODUCT FAMILY

DICE (PRODUCT FAMILY)

PACKAGE TYPE A212KS

PAINTING:

LEAD CUTTING:

REF. DOCUMENTS:

1 input A	6 output A
2 ground	5 collector
3 input B	4 output B

REVISIONS

1108A07
CLW 3/25/68

APPROVED/DATE
Paul Greif

NO.

PAGE of